Amendments to the Specification

Please amend paragraph [0036] of the specification as follows:

In the 720 pixel per line example set forth above, rate controller 316 could initially set the divisor value to 720. If slave pulse stream 305 starts to lag master pulse stream 303, this will be detected by digital comparator 312 which would increase the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will decrease the divisor to a value of, say, 710. This will cause pulses from divider 318 to arrive at phase detector 304 sooner than before. This, in turn, will cause VCO [[306]] 308 to slow down, effectively decreasing the response time of the loop. Similarly, if slave pulse stream 305 starts to lead master pulse stream 303, this will be detected by digital comparator 312 which would decrease the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will increase the divisor to a value of, say, 730. This will cause pulses from divider 318 to arrive at phase detector 304 later than before. This, in turn, will cause VCO [[306]] 308 to speed up, effectively increasing the response time of the loop.

Please amend paragraph [0015] of the specification as follows:

Another aspect of the invention is the phase-locked loop circuit having a digital rate controller. The digital rate control feature allows the phase-locked loop to be programmable so that its speed can be adjusted to react more ~~more~~ quickly or more slowly to changes.